2811

500.32049R00

#10 IDS
4-4-01
R. Drake

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: KAJIHARA et al.

Serial No.: 09/328,910

Filed: June 9, 1999

For: LEADFRAME SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE USING THE SAME, AND METHOD OF AND PROCESS FOR FABRICATING THE TWO

Art Unit: 2811

Examiner: unassigned

INFORMATION DISCLOSURE STATEMENT
WITHIN 3 MONTHS OF FILING OR BEFORE FIRST ACTION
WITH FORM PTO-1449(s)

Assistant Commissioner
for Patents
Washington, D.C. 20231

January 22, 2001

Sir:

In the matter of the above-identified application, Applicant is submitting herewith the enclosed item(s) listed in the enclosed Form(s) PTO-1449 for the Examiner's consideration within 3 months of the application's filing date OR before first action on the merits (whichever event occurs last).

For any item not in the English language, a concise explanation of relevance is provided by an English language abstract document provided herewith.

It is respectfully requested that this Information Disclosure Statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (referencing Case No. 500.32049R00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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Attachments:
communication from foreign patent office
copy of each art reference
English language abstract(s)
Form(s) PTO-1449

LIST OF CITED REFERENCES

Date of the Office Action: November 16, 2000
Date of the Search Report:
Date on which the Office Action or Search Report
was received at our office:
Date of :

List of Cited References:

1. Japanese Patent Laid-Open No. 4-67663

2. Japanese Patent Laid-Open No. 3-014262

Remarks:

As to No. 1 and 2, we are enclosing the English abstracts thereof.